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SHEET 1 OF 1

Form PTO 1449 (Modified)		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY DOCKET NO. 248647US2S CONT		SERIAL NO. New Application	
LIST OF REFERENCES CITED BY APPLICANT				APPLICANT Koji SAKUI			
				FILING DATE Herewith 2/11/04		GROUP	
				U.S. PATENT DOCUMENTS			
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
Gu	AA	6,434,034	08/2002	Wallace et al.	—	—	
Gu	AB	6,278,616	08/2001	Gelsomini et al.	—	—	
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OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, etc.)							
Gu	AE	Yoshihisa IWATA, et al. "A 35 ns CYCLE TIME 3.3 V ONLY 32 Mb NAND FLASH EEPROM," IEEE Journal of Solid-State Circuits, Vol. 30, No. 11, November 1995, pgs 1157-1164.					
	AF	Toru TANZAWA, et al. "A COMPACT ON-CHIP ECC FOR LOW COST FLASH MEMORIES," IEEE Journal of Solid-State Circuits, Vol. 32, No. 5, May 1997, pgs, 662-669.					
	AG	Hitoshi KUME, et al. "A 1.28 $\mu$ m <sup>2</sup> CONTACTLESS MEMORY CELL TECHNOLOGY FOR A 3V-ONLY 64Mbit EEPROM," IEDM Technology Digest, December 1992, 92 pgs, 991-993.					
	AH	Hitoshi MIWA, et al. "A 140mm <sup>2</sup> 64Mb AND FLASH MEMORY WITH A 0.4 $\mu$ m TECHNOLOGY," IEEE International Solid-State Circuits Conference, ISSCC Digest of Technical Papers, February 1996, pgs, 34-35.					
	AI	H. ONODA, et al. "A NOVEL CELL STRUCTURE SUITABLE FOR A 3.VOLT OPERATION, SECTOR ERASE FLASH MEMORY," IEDM Technology Digest, December 1992, pgs. 599-602.					
	AJ	S. KOBAYASHI, et al. "A 3.3 V-ONLY 16Mb DINOR FLASH MEMORY," ISSCC Digest of Technical Papers, February 1995, pgs, 122-123.					
	AK	F. MASUOKA, ET AL. "A NEW FLASH E <sup>2</sup> PROM CELL USING TRIPLE POLYSILICON TECHNOLOGY: IEDM Technology Papers, February 1987, pgs. 76-77.					
	AL	Georgha SAMACHISA, et al. "A 128k FLASH EEPROM USING DOUBLE POLYSILICON TECHNOLOGY" ISSCC Digest of Technical Papers, 1987, pgs. 76-77.					
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	AN	Fujio MASUOKA, et al. "NEW ULTRA HIGH DENSITY EPROM AND FLASH EEPROM WITH NAND STRUCTURE CELL," IEDM 1987, PGS, 552-555.					
	AO	Jin-ki KIM, et al. "A 120-mm <sup>2</sup> 64 Mb NAND FLASH MEMORY ARCHIEVING 180 ns/BYTE EFFECTIVE PROGRAM SPEED," IEEE Journal of Solid-State Circuits, Vol. 32, No. 5, May 1997, pgs. 670-680.					
	AP	Masataka KATO, et al. "A 0.4 $\mu$ m <sup>2</sup> SELF-ALIGNED CONTACTLESSMEMORY CELL TRCHNOLOGY SUITABLE FOR 256-Mbit FLASH MEMORIES," IEDM Technology Digest, 1994, pgs. 921-923.					
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							<input type="checkbox"/> Additional References sheet(s) attached
Examiner Vu Le					Date Considered 7/20/04		
*Examiner: Initial if reference is considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.							